**National Institute Of**

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**Assignment**

**Of**

**VLSI Circuit Design**

# Topic: NMOS and PMOS Characteristics (transfer and output characteristics) aNd analysis

**Submitted To:**

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## **Department: ECE**

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## **Course Code: EC – 401**

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Aim: The aim of this experiment is NMOS and PMOS Characteristics (transfer and output characteristics) and analysis using Cadence simulation software

**Tools Used**: Cadence Software

### Introduciton

Transistors are fundamental components in modern electronic devices, serving as building blocks for switching and amplification. NMOS (n-channel MOSFET) and PMOS (p-channel MOSFET) transistors are two types of metal-oxide-semiconductor field-effect transistors (MOSFETs) that operate based on different semiconductor doping types. NMOS devices are constructed with n-type material, resulting in electrons as the majority charge carriers, while PMOS devices use p-type materials, with holes as the majority charge carriers.

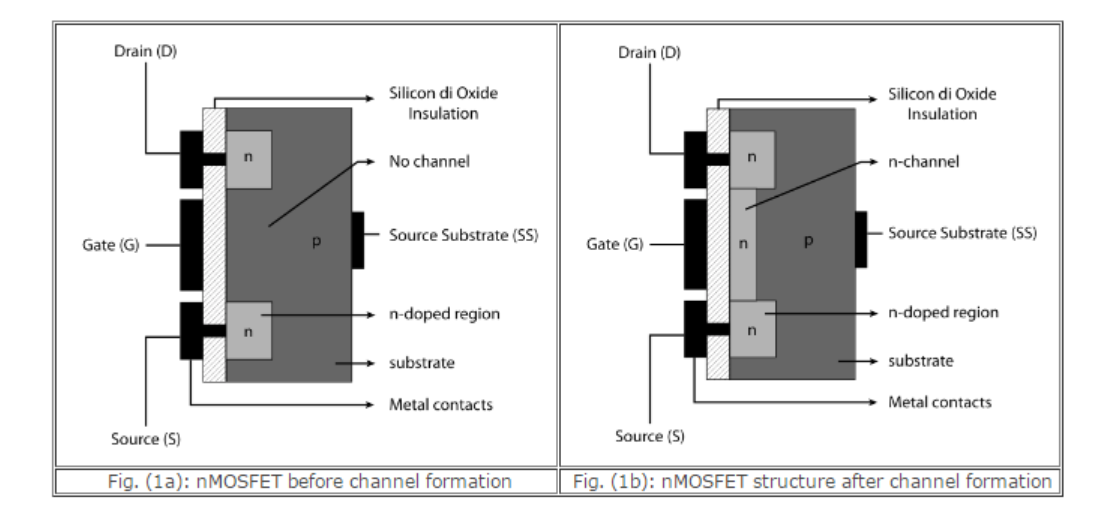


Fig: nmos before and after channel formation

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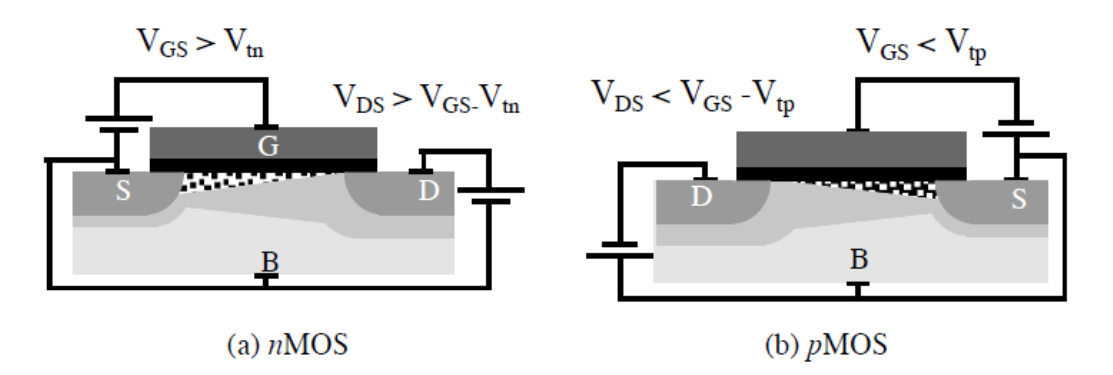


Fig: Circuit symbol for nmos and pmos

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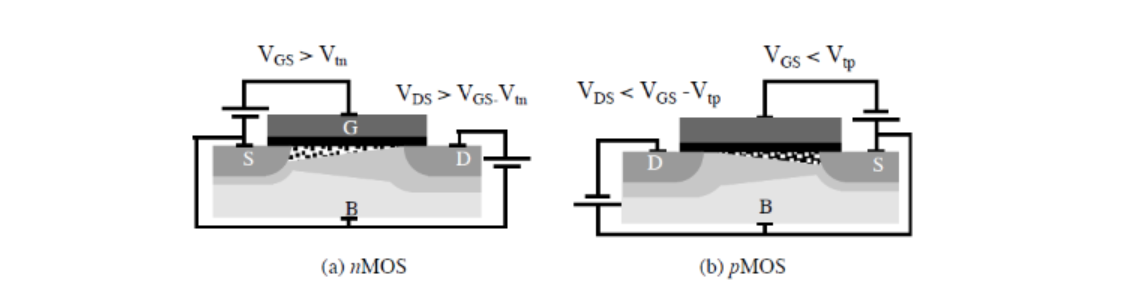


Fig: Channel pinchoff for nmos and pmos

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The characterization of NMOS and PMOS devices is critical in integrated circuit design, as it influences performance metrics such as speed, power consumption, and thermal stability. The transfer characteristic reflects how the output current varies with the input voltage, while the output characteristic reveals the relationship between output current and output voltage at different gate-source voltages. This experimental investigation aims to provide comprehensive insights into these characteristics to enhance understanding and application in electronic circuits.

|  |  |  |  |
| --- | --- | --- | --- |
| Kind of MOSFET | Region of Operation | | |
|  | **Cut-Off** | **Ohmic/Linear** | **Saturation** |
| n-channel Enhancement-type | VGS < VT | VGS > VT and VDS < VP | VGS > VT and VDS > VP |
| p-channel Enhancement-type | VGS > -VT | VGS < -VT and VDS > -VP | VGS < -VT and VDS < -VP |
| n-channel Depletion-type | VGS < -VT | VGS > -VT and VDS < VP | VGS > -VT and VDS > VP |
| p-channel Depletion-type | VGS > VT | VGS < VT and VDS > -VP | VGS < VT and VDS < -VP |

Table: Region of Operation for different type of Mosfet

### nmosVC​(t)=Vin​e−RCt​

**NMOS (N-type MOSFET):**

* The NMOS transistor turns on when a positive voltage is applied to the gate relative to the source.
* The current flows from the drain to the source when the transistor is in the active region

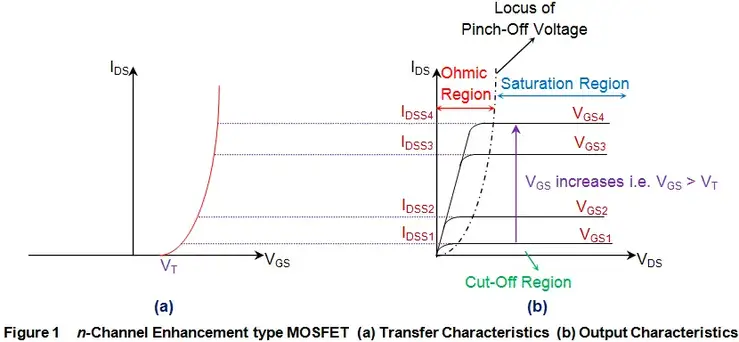


Fig: Nmos and Pmos (a) Input (b) Output Characterstics

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**1. Transfer Characteristics:**

The transfer characteristics of an NMOS transistor describe the relationship between the gate-source voltage (Vgs​) and the drain current (Id​).

The drain current Id​ in the saturation region is given by:

where:

* k is the process transconductance parameter.
* W is the width of the transistor.
* L is the length of the transistor.
* V{th}Vth​ is the threshold voltage.

**2. Output Characteristics:**

In the saturation region, the output characteristics of the NMOS transistor are described by:

where λ is the channel-length modulation parameter.

### Pmos

**1. Transfer Characteristics:**

For a PMOS transistor, the drain current IDI\_DID​ in the saturation region is:

where:

* Vsg​ is the source-gate voltage.
* ∣Vth∣ is the magnitude of the threshold voltage.

2. Output Characteristics:

In the saturation region, the output characteristics for the PMOS transistor are:

ϕ(f)=−arctan(2πfRC)

### circuit Design

1. **NMOS:**

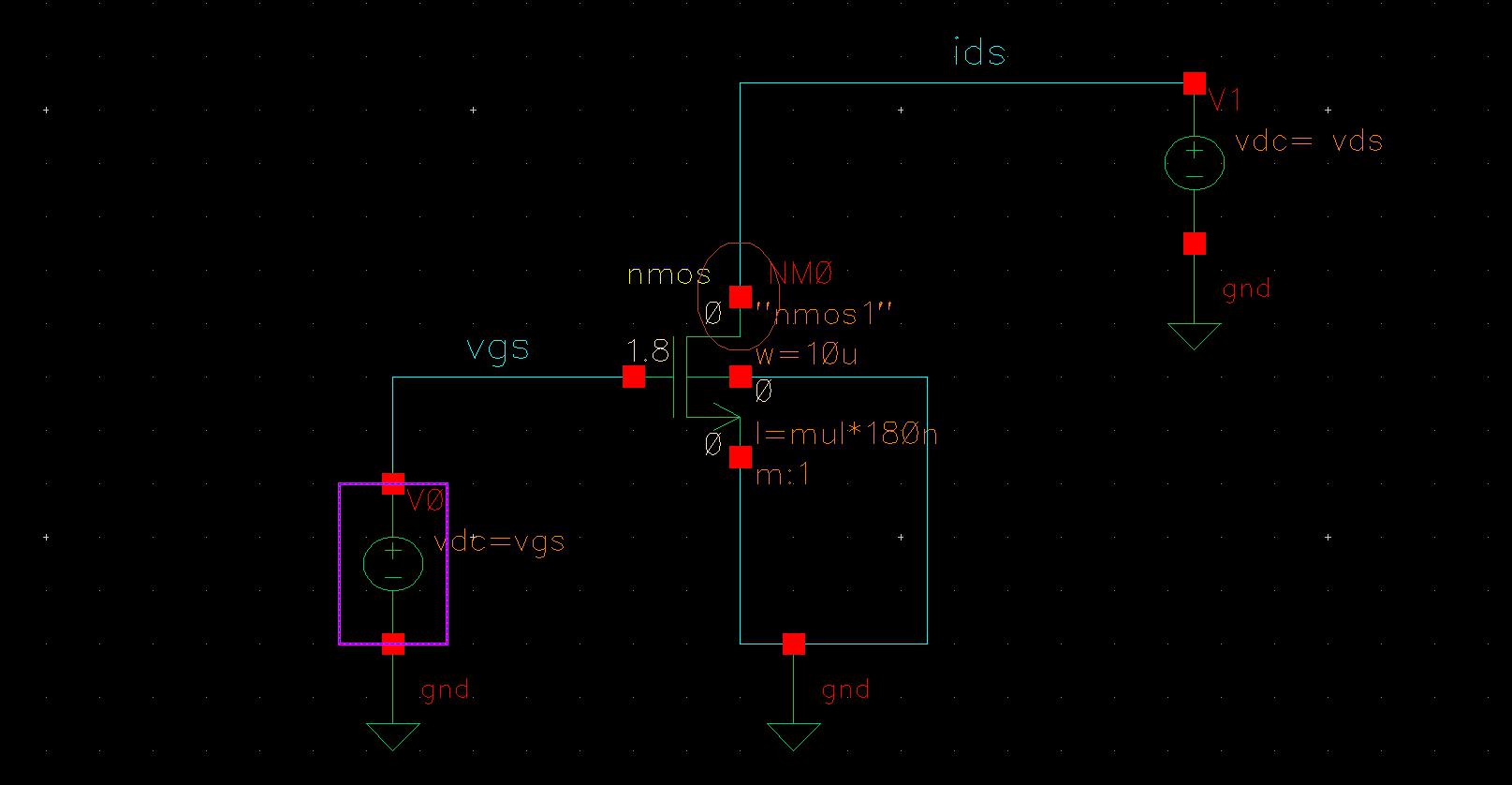


Fig: Circuit Diagram NMOS

* **Transfer Characteristics**

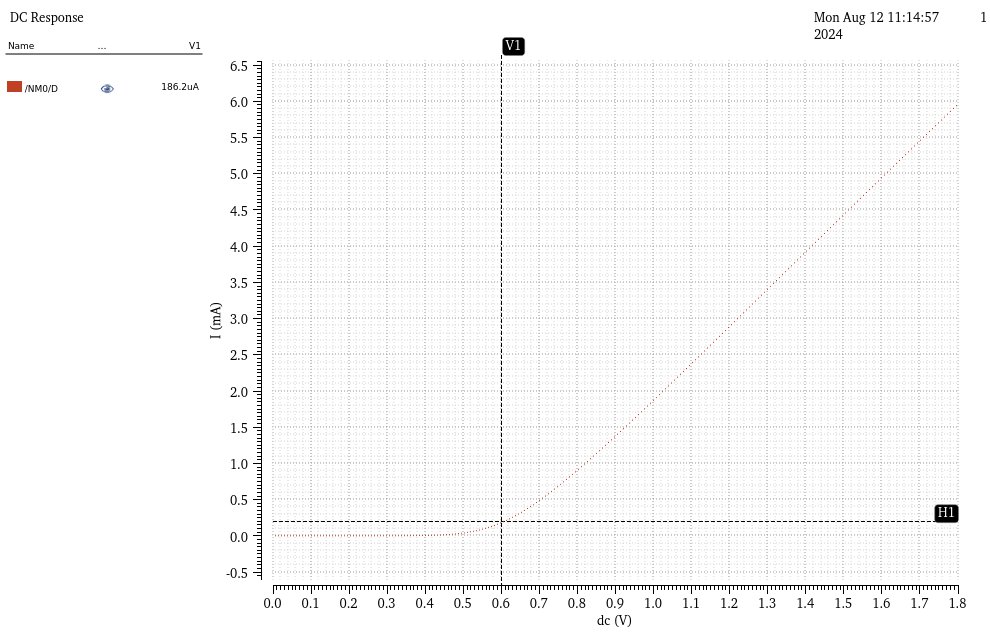


Fig: Id​ versus Vgs for NMOS

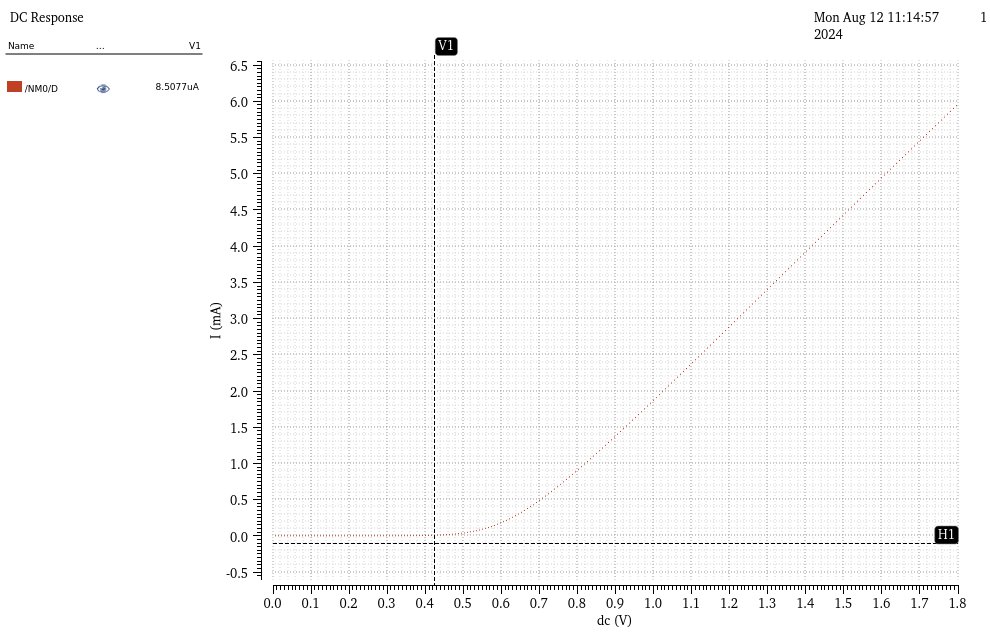


Fig: Id​ versus Vgs for different vds ( NMOS)

1. **PMOS:**

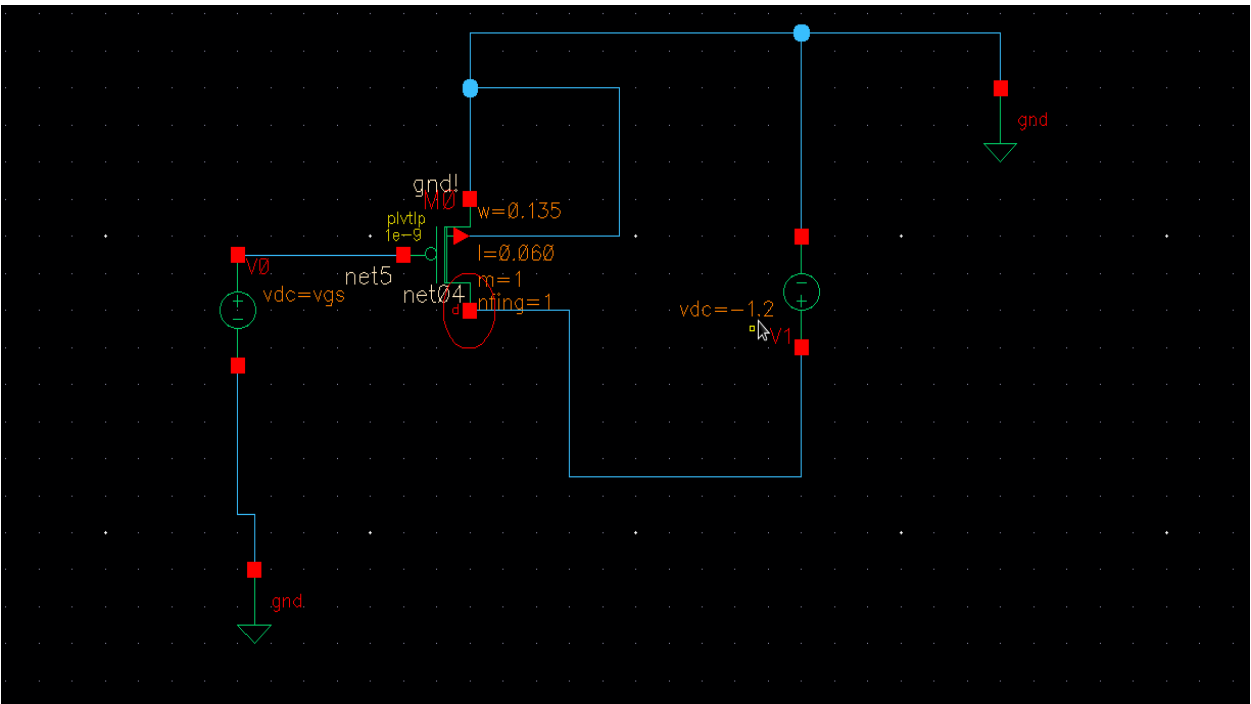


Fig: Circuit Diagram PMOS

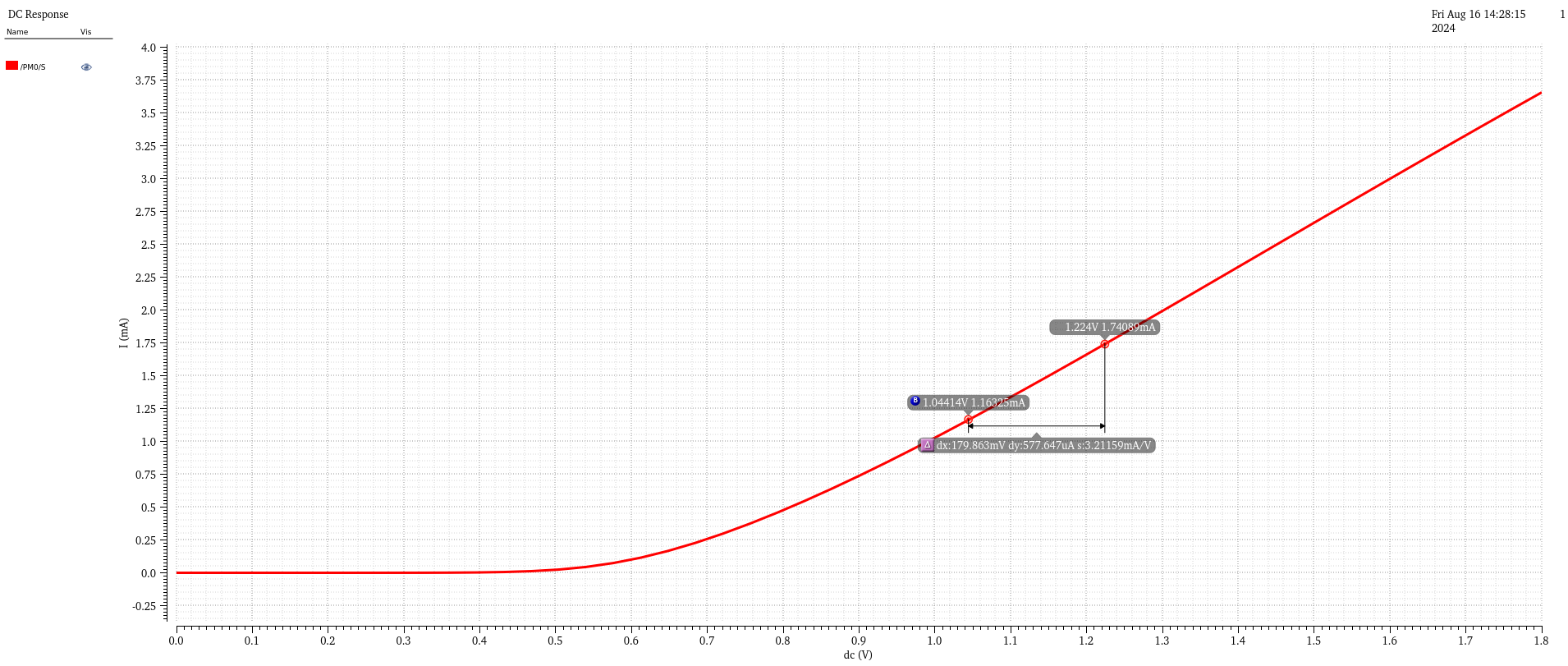


Fig: Ids versus Vsg for Vsd > Vth and calutation of Slope

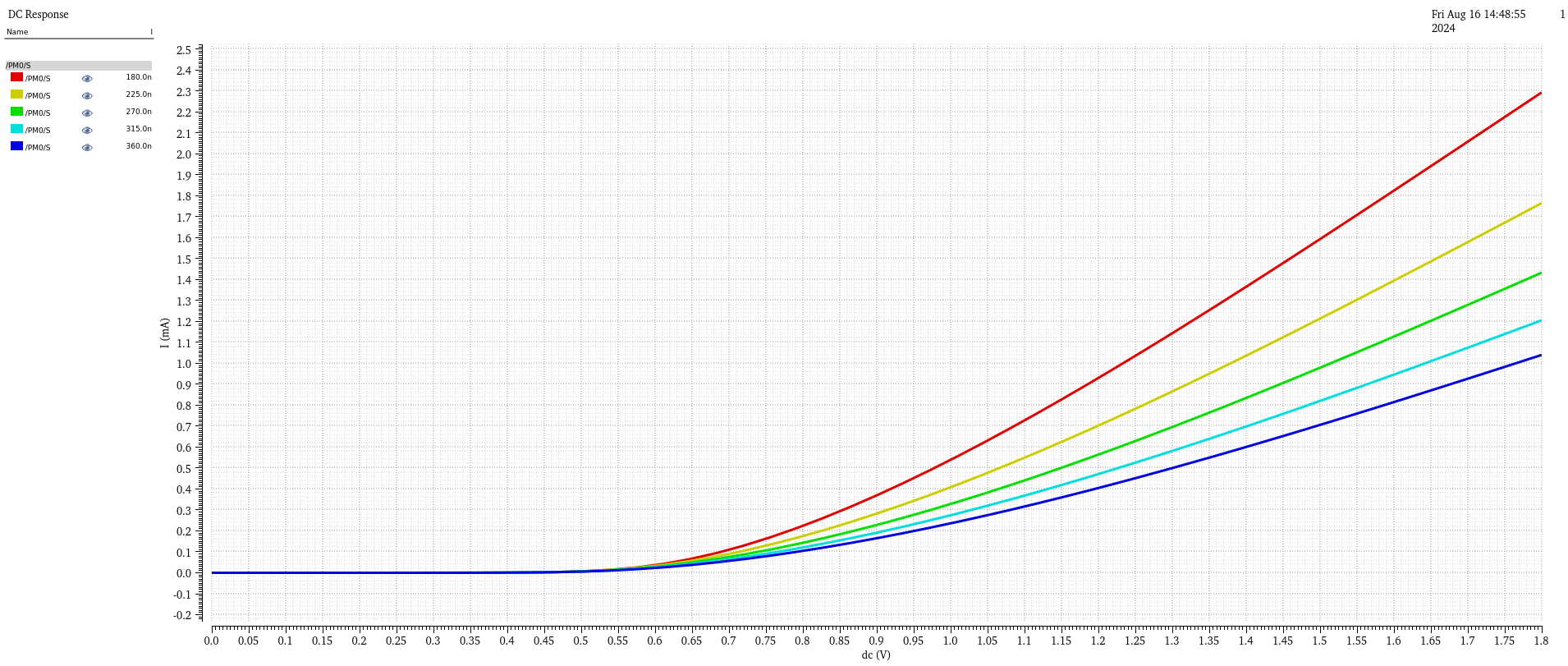


Fig: Ids versus Vsg for different values of Vsd > Vth

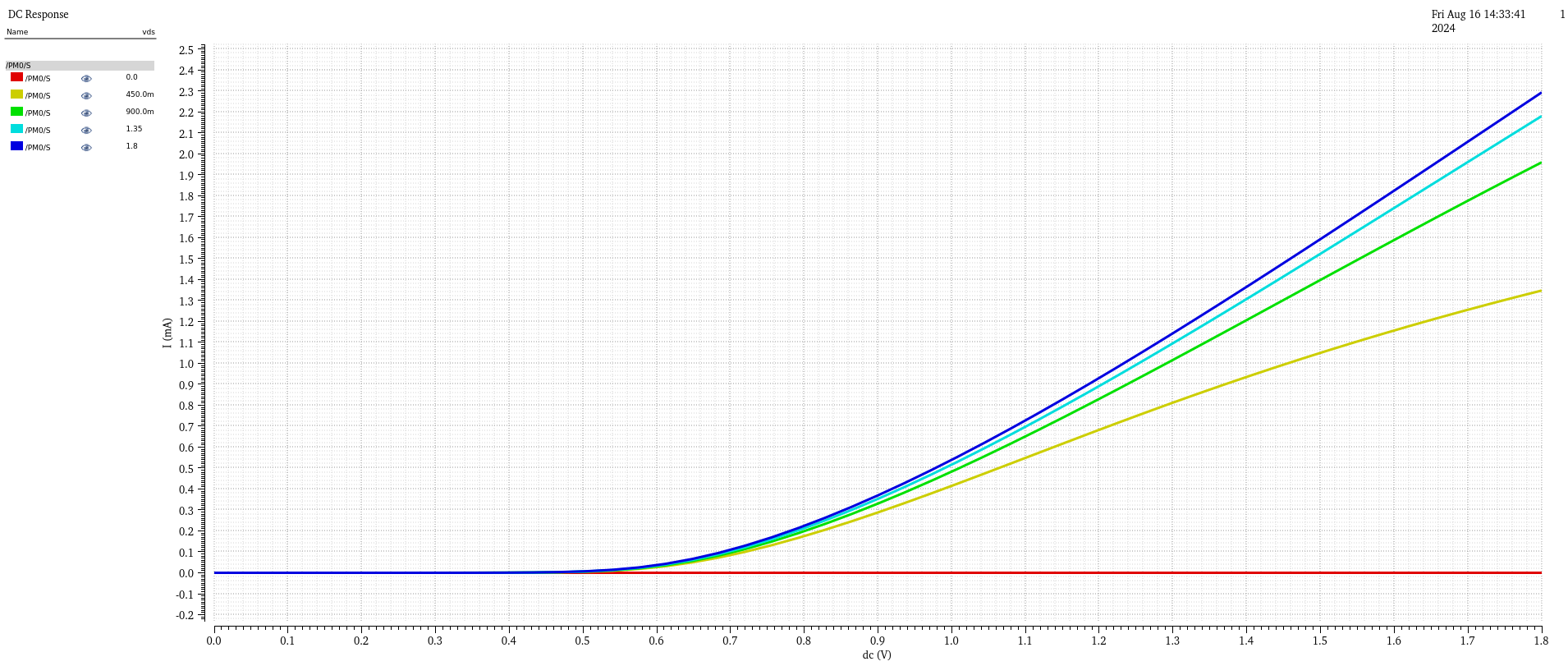


Fig: Ids versus Vsg for different values of Vsd > Vth and Vsd < Vth

* **Output Characteristics**

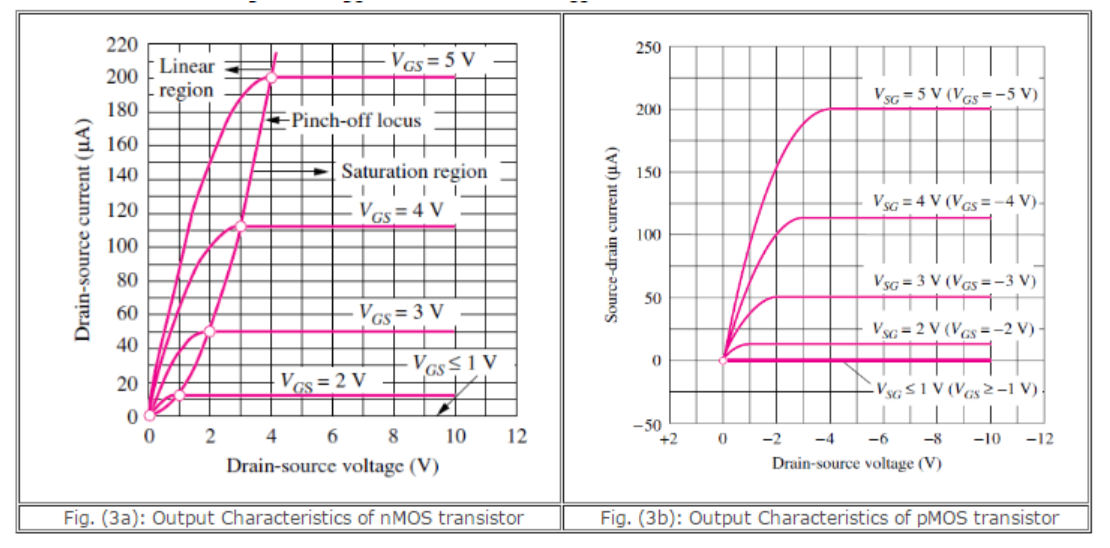
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Fig: Output Charcterstics (a) Nmos (b) PMOS

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1. **NMOS:**

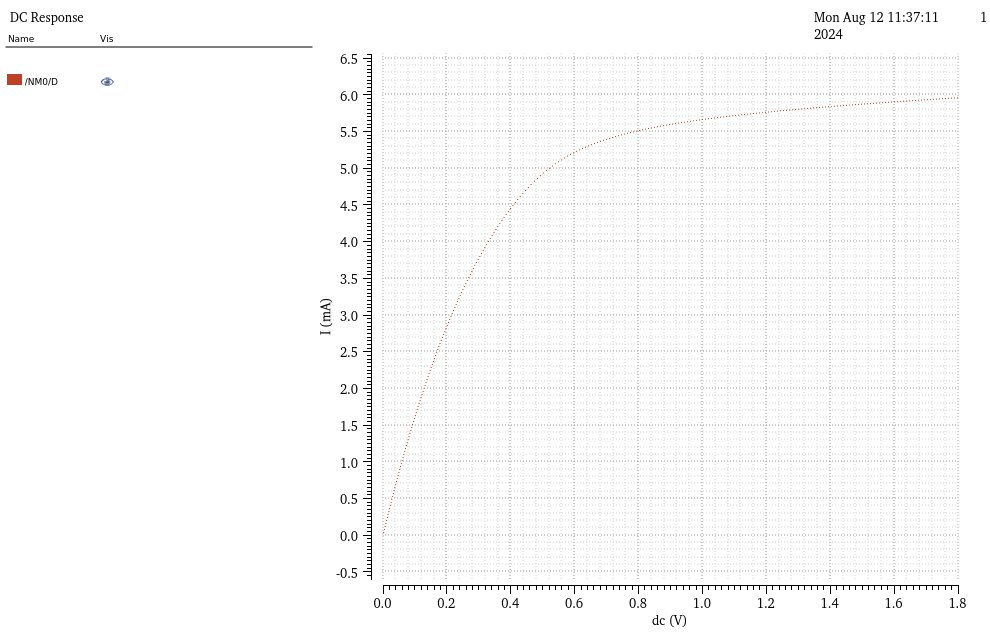


Fig: Id​ versus Vds NMOS

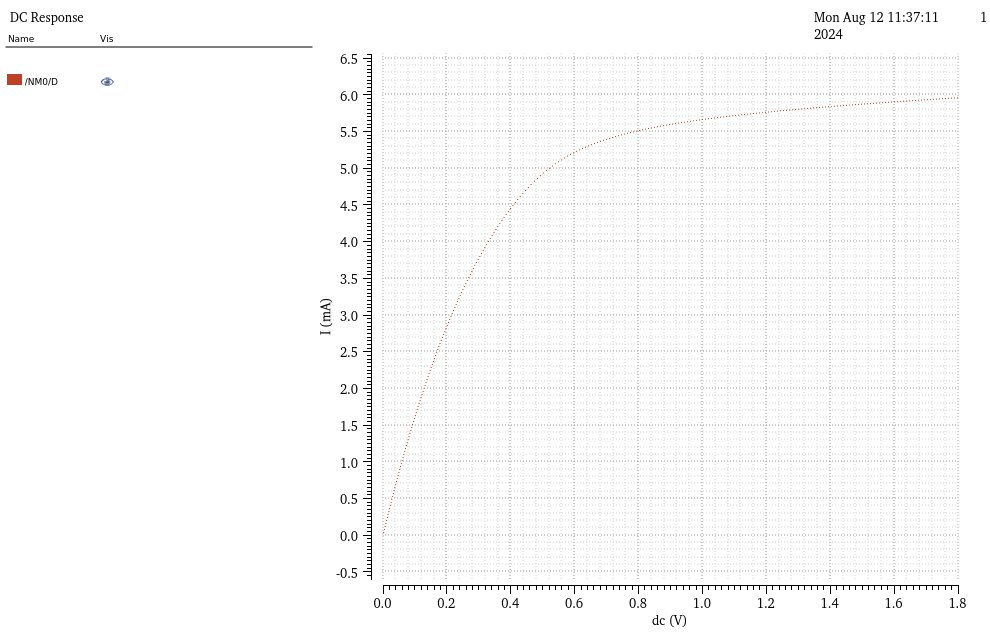


Fig: Id​ versus Vds for different vgs (NMOS)

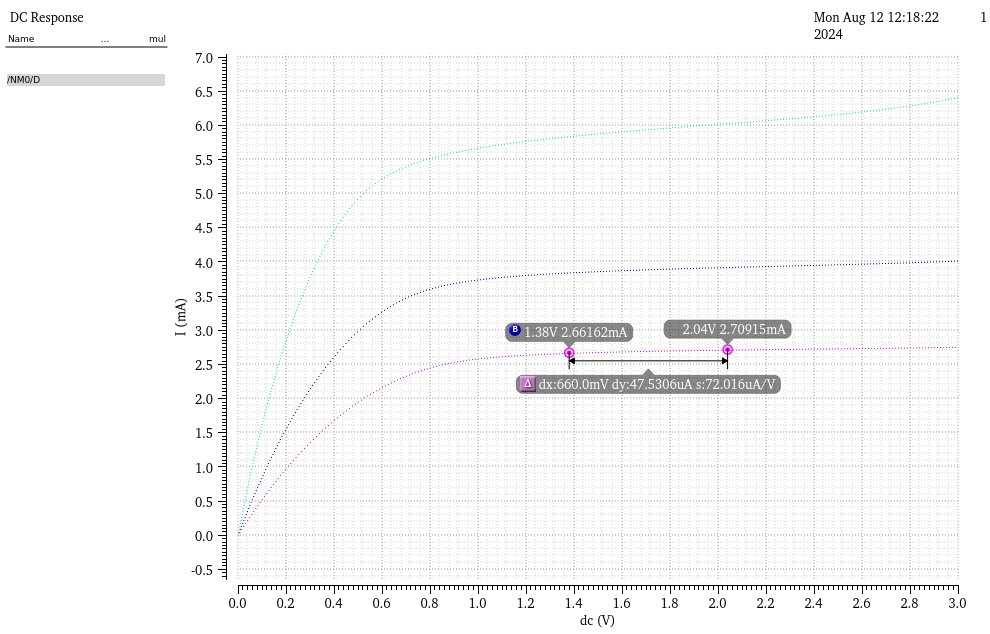


Fig: Id​ versus Vds for different vgs and length varition (NMOS)

1. **PMOS:**

* Plots Id​ versus Vsd​ for different Vsg values.

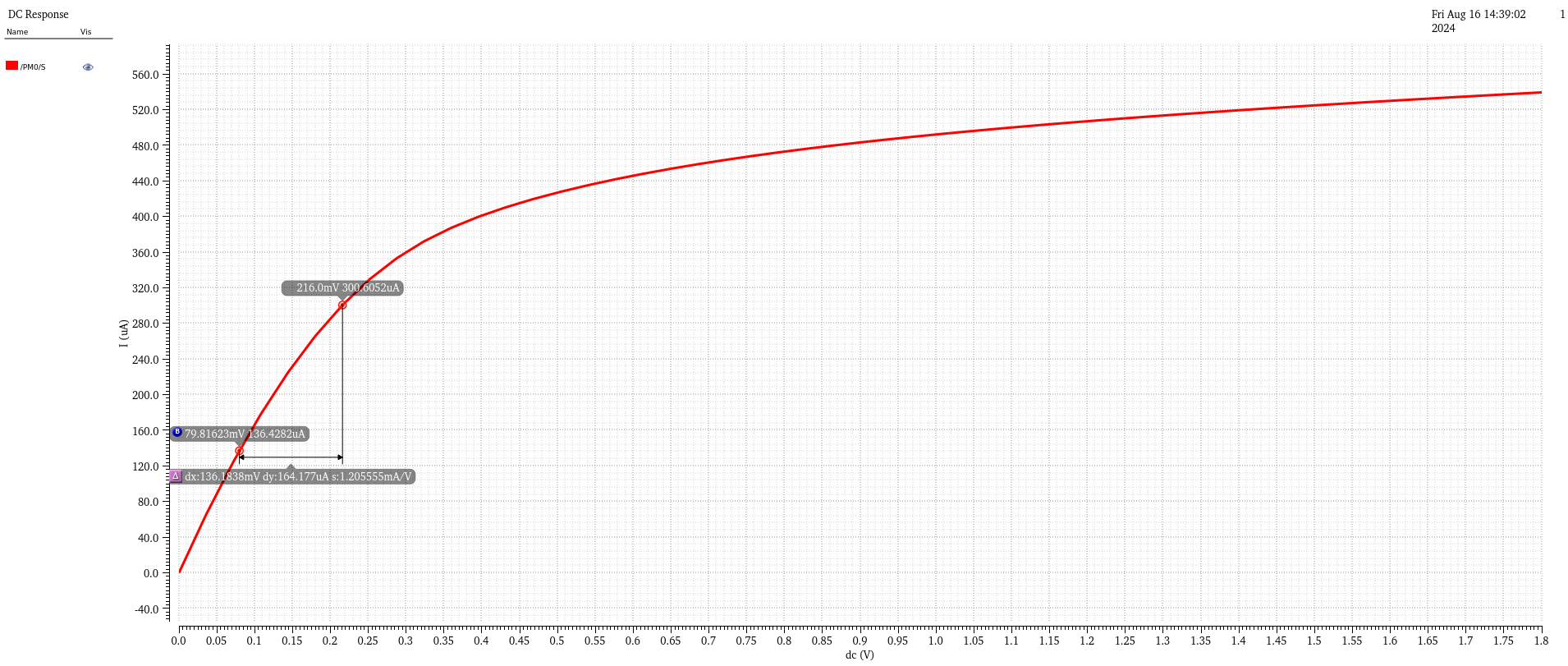


Fig: Ids versus Vsd​ for vgs > Vth

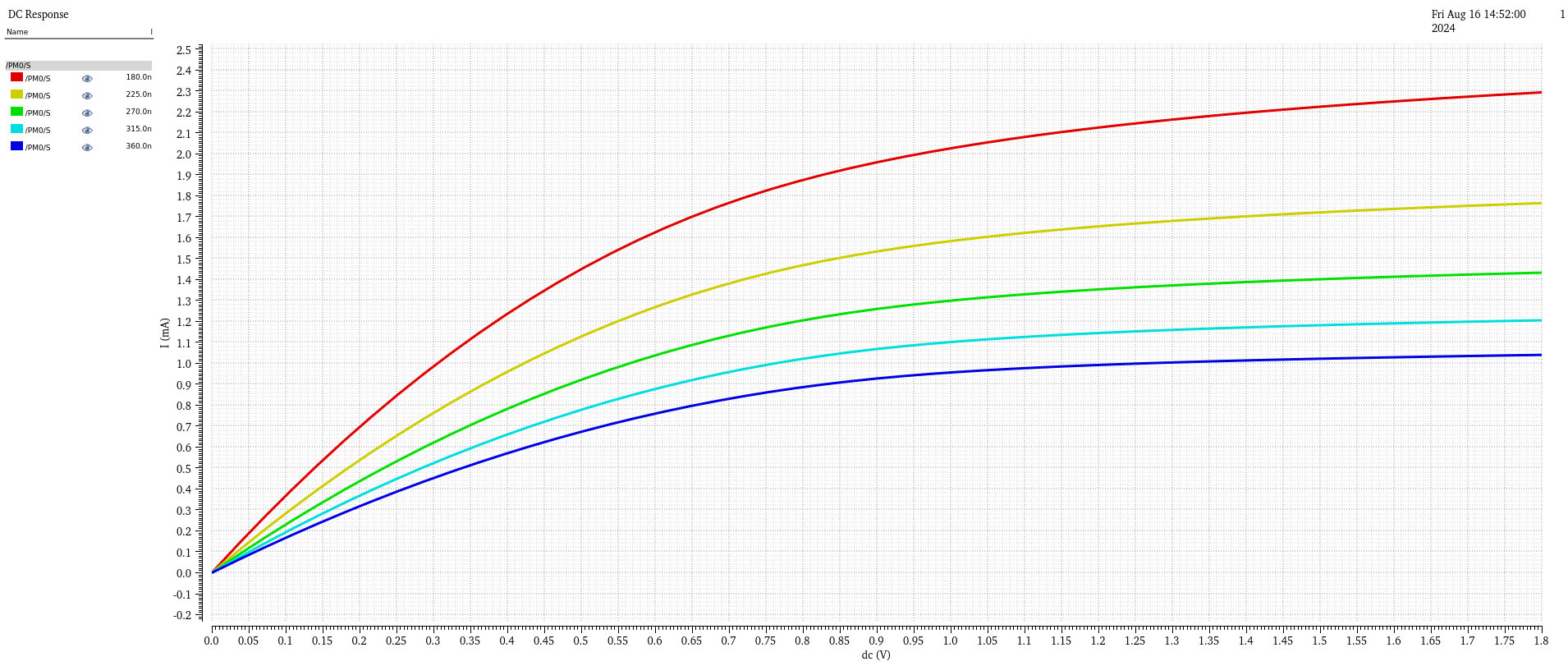


Fig: Ids versus Vsd​ for different value of vsg

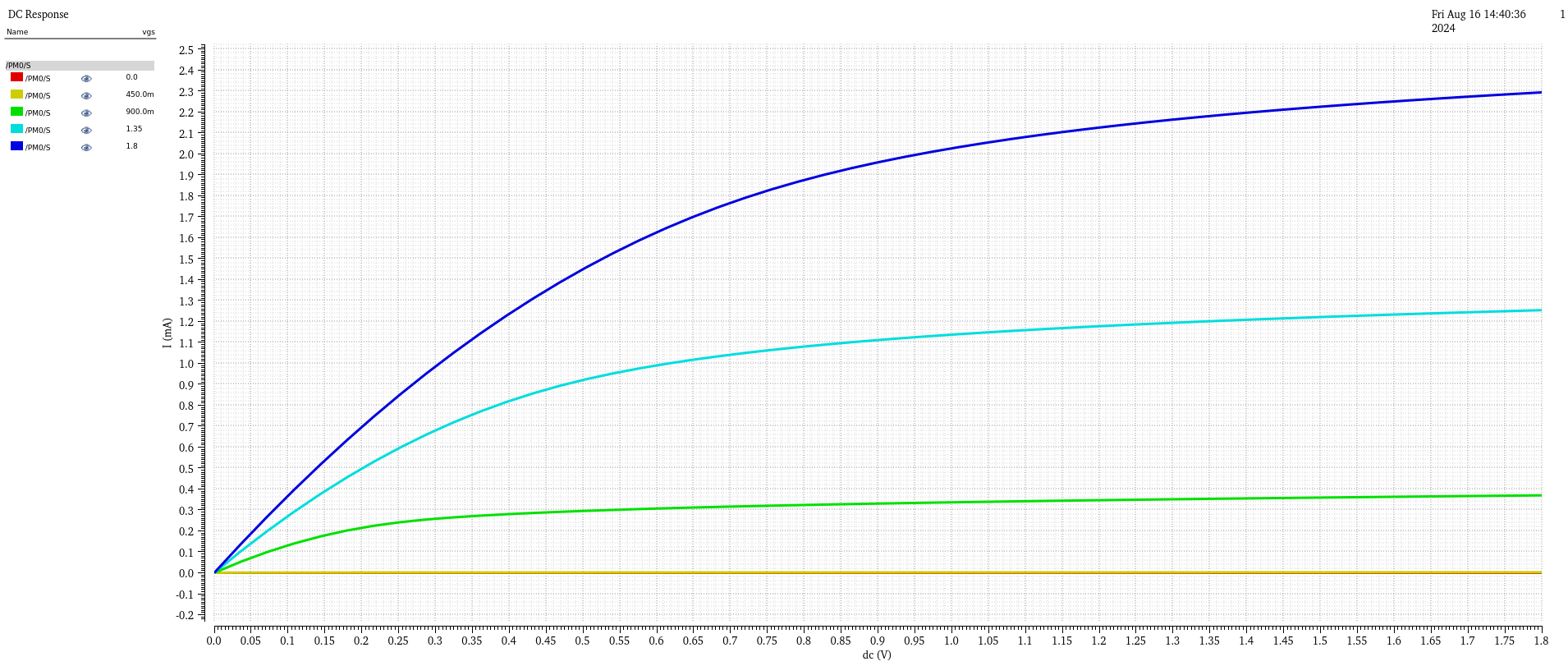


Fig: Ids versus Vsd​ for different value of vsg

### procedure

**1. Setup in Cadence:**

1. Open Cadence Virtuoso and create a new schematic for the NMOS and PMOS transistor circuits.
2. Add an NMOS transistor and a DC voltage source for VGS​ and VDS​.
3. Repeat the setup for the PMOS transistor with appropriate polarity for the voltage sources.
4. Connect the measurement probes to record the drain current Id and the gate voltage Vgs or Vsg​.

**2. Simulation of Transfer Characteristics:**

1. Set Vds​ to a constant value (e.g., 1.8V for NMOS and -1.8V for PMOS).
2. Sweep Vgs​ from 0V to the supply voltage for NMOS (or from 0V to the negative supply voltage for PMOS).
3. Run the simulation and plot Id versus Vgs​ to obtain the transfer characteristics.

**3. Simulation of Output Characteristics:**

1. Set Vgs​ to a constant value above the threshold voltage (e.g., 2.5V for NMOS and -2.5V for PMOS).
2. Sweep Vds​ from 0V to the supply voltage for NMOS (or from 0V to the negative supply voltage for PMOS).
3. Run the simulation and plot Ids versus Vds to obtain the output characteristics.

### Observations

1. **NMOS Transfer Characteristics:**
   * Threshold voltage Vth​ observed at approximately 0.7V.
   * Drain current ID​ increases quadratically with Vgs​ beyond Vth​.
2. **PMOS Transfer Characteristics:**
   * Threshold voltage Vth​ observed at approximately -0.7V.
   * Drain current ID​ increases quadratically with |VSG​∣ beyond |Vth​∣.
3. **NMOS Output Characteristics:**
   * In the linear region, ID​ increases linearly with Vds​.
   * In the saturation region, ID​ remains constant as Vds ​ increases.
4. **PMOS Output Characteristics:**
   * Similar behaviour to NMOS but with polarities reversed.
   * Id​ remains constant in the saturation region, decreases linearly in the linear region.

**1. Extracting NMOS Mobility (​):**

To determine the electron mobility for the NMOS transistor, use the following formula:

Where:

* Id is the drain current.
* is the oxide capacitance per unit area.
* ​ is the width-to-length ratio of the transistor.
* ​ is the gate-to-source voltage.
* is the threshold voltage.

**2. Extracting PMOS Mobility (​):**

For the PMOS transistor, the hole mobility is determined by:

Where:

* Id is the drain current.
* ​ is the oxide capacitance per unit area.
* ​ ​ is the width-to-length ratio of the transistor.
* VSG​ is the source-to-gate voltage.
* is the absolute value of the threshold voltage.

**3. Extracting Threshold Voltage ( ​):**

The threshold voltage can be extracted from the transfer characteristics using:

Where:

* Id is the drain current.
* is the electron mobility.
* is the oxide capacitance per unit area.
* is the width-to-length ratio of the transistor.
* ​ is the gate-to-source voltage.

**Example Calculations:**

1. **NMOS Mobility ():**

Suppose the following values are obtained from the simulation:

* + Drain current Id=2 mA
  + Gate-to-source voltage VGS=2.5 V
  + Threshold voltage Vth=0.7 V
  + Width-to-length ratio
  + Oxide capacitance Cox =1 fF/µm2 C

Plugging these values into the equation:

**2.PMOS Mobility (​):**

Assume similar values for the PMOS:

* Drain current ID=2 mA
* Source-to-gate voltage VSG=−2.5
* Threshold voltage ∣Vth∣=0.7 V
* Width-to-length ratio
* Oxide capacitance Cox =1 fF/µm2 C

Using the equation:

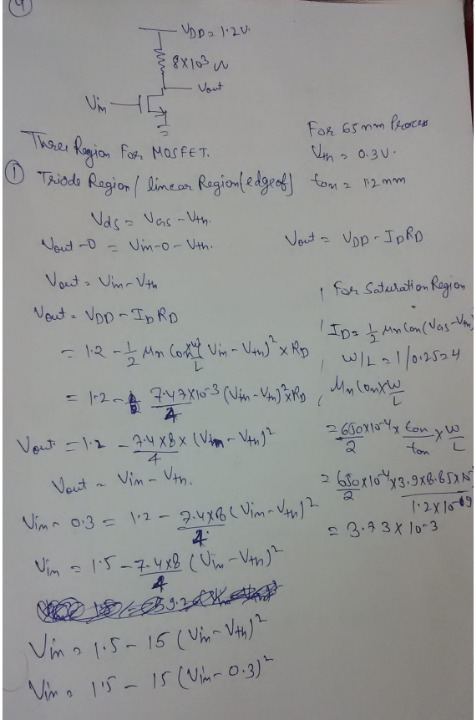
**3.Threshold Voltage Extraction (​):**

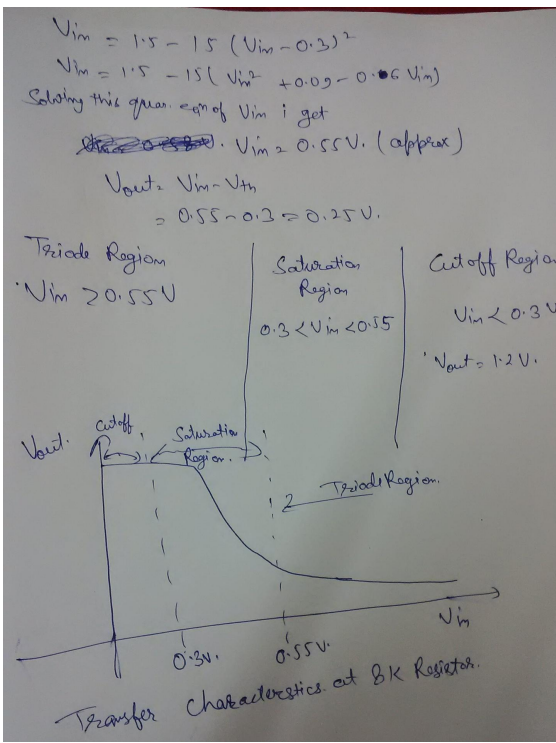
From simulation data:

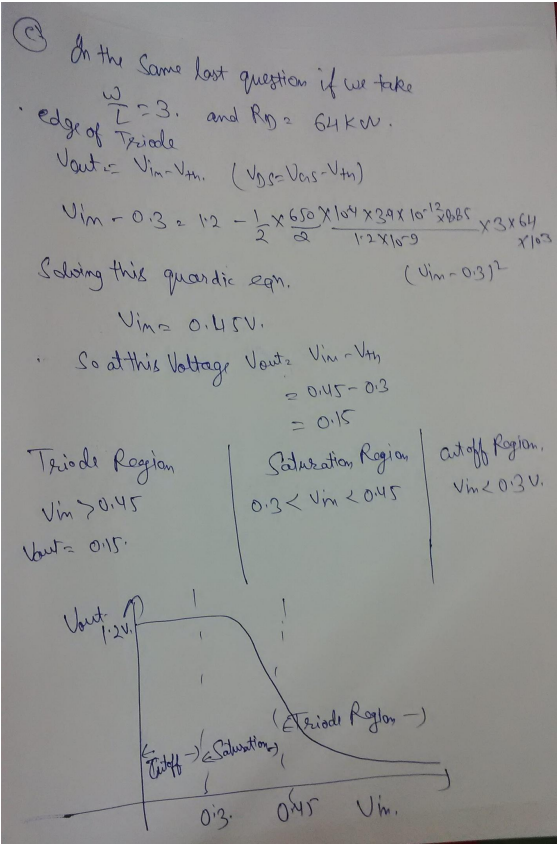
* Gate-to-source voltage VGS=2.5 V
* Drain current ID=2 mA
* Mobility μn=1.23×103 cm2/Vs
* Width-to-length ratio W\L=10
* Oxide capacitance Cox=1 fF/µm2

Calculating VthV\_{th}Vth​:

### Theoritical calculation







### conclusion

The experiment successfully demonstrated the transient and AC responses of an RC circuit using Cadence simulation software. The results for the transient response matched theoretical expectations, confirming the accuracy of the time constant and capacitor behaviour. The AC response analysis also aligned well with theoretical predictions, providing insights into the circuit's frequency response. The experiment reinforced the understanding of RC circuit dynamics and the utility of simulation tools in circuit analysis.

# References

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2. Sung –Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits- Analysis & Designing”, MGH, Third Ed., 2003

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